



We take research and
our employees to the
next level.

Change starts with us.

System on Chip (SoC) Verification Engineer (all genders)

The [Fraunhofer-Gesellschaft](#) currently operates 76 institutes and research institutions throughout Germany and is the world's leading applied research organization. Around 32 000 employees work with an annual research budget of 3.4 billion euros. The Fraunhofer Institute for Integrated Circuits IIS, located in Erlangen, is the largest institute of the Fraunhofer-Gesellschaft with more than 1 200 employees.

We bring chip design back to Europe!

For a technologically more independent Europe, we aim to develop Fraunhofer IIS into a European IC Design Center for trusted and energy-efficient high-speed ICs by 2026. As a leading competence center for digital chip design, we deliver essential cutting-edge technologies in the areas of exascale high-performance computing and trusted electronics. In addition, we offer sophisticated digital design services based on RISC-V. Our target customers are design houses, semiconductor manufacturers, SMEs, and system integrators. Potential applications are areas such as high-speed data processing, blockchain or cybersecurity. Today, our [»Integrated Digital Systems«](#) business unit develops digital circuits in CMOS technologies as System on Chip, ASIC or IP.

Here's how you will make a difference

As a SoC Verification Engineer, you will play a key role in pre-silicon RTL verification of block and top-level SoC designs utilizing RISC-V architecture. Working closely with cross-functional teams, you will help shape a modern, reusable verification environment using state-of-the-art methodologies and metric-driven approaches.

Your key responsibilities:

- Understand the nuances of RISC-V architectures and industry-standard low-power architectures to build block/chip level testbenches using best-in-class verification methodologies
- Translate design specifications into comprehensive verification plans in collaboration with system architects
- Develop and maintain reusable testbenches for IP/block-level verification and support IP integration verification
- Create smart, constraint-random and directed test cases tailored to RISC-V SoCs
- Build and analyze coverage models, and refine tests to close coverage gaps
- Debug test failures, manage bug tracking, and ensure coverage closure
- Lead verification reviews to uphold coding quality and best practices in SoC verification
- Prepare, run, and evaluate regression runs

What you bring to the table

- University degree in (electrical) engineering, IT/computer science or another related field
- Solid understanding of digital logic design and RISC-V-based SoC architecture
- Proven experience with SystemVerilog and UVM-based verification environments
- Very good English and good German language skills
- Proactive and independent mindset

Nice to have

- Familiarity with C / C++ programming, assembly and object-oriented languages such as Python
- Knowledge of industry-standard interfaces and bus protocols (e.g., AXI)
- Experience with IP verification methods, integration verification specific to RISC-V and embedded CPU verification
- Interest in low power verification techniques and formal verification tools (e.g. JasperGold)

What you can expect

Fraunhofer is not only the largest organization for applied research in Europe, but also a top-rated employer. How so?

- **Our institute culture:** We want our colleagues to feel comfortable. Therefore, we constantly strive to ensure a friendly and supportive working atmosphere within our international team.
- **Exciting activities:** With customers and partners across the globe, we provide an attractive working environment in a highly innovative key industry with exciting ventures and new experiences.
- **Room for creativity:** We want to give our colleagues a generous amount of creative freedom so that they can contribute and develop their own ideas.
- **Personal development:** With top-of-the-range company equipment and regular training, we aim to provide the best possible working conditions and development opportunities for our colleagues.
- **Flexible working hours:** Due to our wide range of offers, we make it easy for our colleagues to find a comfortable balance between their private and professional lives.

The position is initially limited to 2 years with the aim to extend it subsequently. The weekly working time is 39 hours. The position can also be filled on a part-time basis with a preference, however, to have it filled as close to a full-time position as possible.

We value and promote the diversity of our employees' skills and therefore welcome all applications - regardless of age, gender, nationality, ethnic and social origin, religion, ideology, disability, sexual orientation and identity. Appointment, remuneration and social security benefits based on the public-sector collective wage agreement (TVöD).

With its focus on developing key technologies that are vital for the future and enabling the commercial utilization of this work by business and industry, Fraunhofer plays a central role in the innovation process. As a pioneer and catalyst for groundbreaking developments and scientific excellence, Fraunhofer helps shape society now and in the future.

Intimidating? Don't worry.

We are an interdisciplinary team, looking to support young career-oriented talents. Hence, do not hesitate to join Fraunhofer and send us your application! Please submit it (cover letter, CV and grade sheets) [online!](#)

Questions about this position will be answered by Luca Prietz.

Fraunhofer Institute for Integrated Circuits IIS

www.iis.fraunhofer.de

Requisition Number: 1951552

Location: Erlangen

